

CLAIMS

1. A semiconductor device, comprising:

a semiconductor substrate;

5 a nonvolatile memory cell that includes

a memory transistor realized by a MOS

transistor including a memory gate oxide film that is arranged

on the semiconductor substrate, and a floating gate made of

polysilicon that is arranged on the memory gate oxide film

10 which floating gate is in an electrically floating state; and

a selection transistor realized by a MOS

transistor that is serially connected to the memory transistor,

the selection transistor including a selection gate oxide film

that is arranged on the semiconductor substrate, and a

15 selection gate made of polysilicon that is arranged on the

selection gate oxide film; and

a peripheral circuit transistor realized by a MOS

transistor including a peripheral circuit gate oxide film that

is arranged on the semiconductor substrate, and a peripheral

20 circuit gate made of polysilicon that is arranged on the

peripheral circuit gate oxide film;

wherein the memory gate oxide film is arranged to

be thinner than the peripheral circuit gate oxide film.

25 2. The semiconductor device as claimed in claim 1,

wherein the memory transistor and the selection transistor are PMOS transistors.

3. The semiconductor device as claimed in claim 1,
5 wherein the selection gate oxide film and the memory gate oxide film are arranged to have a same thickness.

4. The semiconductor device as claimed in claim 1,
wherein the selection gate oxide film and the
10 peripheral circuit gate oxide film are arranged to have a same thickness.

5. The semiconductor device as claimed in claim 1,
further comprising:
15 a capacitor including a lower electrode made of polysilicon that is arranged on the semiconductor substrate via an insulating film, and an upper electrode made of polysilicon that is arranged on the lower electrode via a capacitor insulating film;

20 wherein the floating gate and the lower electrode are created from a same polysilicon layer, and the capacitor insulating film is arranged on an upper surface and a side surface of the floating gate.

25 6. The semiconductor device as claimed in claim 5,

wherein the peripheral circuit gate and the upper electrode are created from a same polysilicon layer.

7. The semiconductor device as claimed in claim 5,
5 wherein the selection gate, the floating gate, and the lower electrode are created from the same polysilicon layer.

8. The semiconductor device as claimed in claim 6,
10 wherein the selection gate, the peripheral circuit gate, and the upper electrode are created from the same polysilicon layer.

9. A semiconductor device, comprising:
15 a divider resistor circuit that is configured to obtain a voltage output through voltage division and adjust the voltage output through cutting one or more fuse elements;
the divider resistor circuit including
a plurality of resistance value adjusting
20 resistor elements the are serially connected;
a plurality of fuse MOS transistors as the fuse elements that are connected in parallel to the resistance value adjusting resistor elements;
a nonvolatile memory cell that includes a
25 memory transistor and a selection transistor, the memory

transistor being realized by a MOS transistor including a
memory gate oxide film that is arranged on a semiconductor
substrate and a floating gate made of polysilicon that is
arranged on the memory gate oxide film which floating gate is
5 in an electrically floating state, and the selection
transistor being realized by a MOS transistor serially
connected to the memory transistor and including a selection
gate oxide film that is arranged on the semiconductor
substrate and a selection gate made of polysilicon that is
10 arranged on the selection gate oxide film; and

a read circuit for switching on/off the fuse
MOS transistors according to the storage state of the
nonvolatile memory cell;

wherein at least one of the fuse MOS transistors
15 and the read circuit is configured as a peripheral circuit
transistor realized by a MOS transistor including a peripheral
circuit gate oxide film that is arranged on the semiconductor
substrate, and a peripheral circuit gate made of polysilicon
that is arranged on the peripheral circuit gate oxide film
20 which peripheral circuit gate oxide film is arranged to be
thicker than the memory gate oxide film.

10. A semiconductor device comprising:

a voltage detecting circuit that includes a divider
25 resistor circuit that divides an input voltage and outputs the

divided voltage, a reference voltage generating circuit that generates a reference voltage, and a comparator circuit that compares the divided voltage from the divider resistor circuit with the reference voltage from the reference voltage

5 generating circuit;

the divider resistor circuit including

a plurality of resistance value adjusting resistor elements that are serially connected;

a plurality of fuse MOS transistors as the
10 fuse elements that are connected in parallel to the resistance value adjusting resistor elements;

a nonvolatile memory cell that includes a memory transistor and a selection transistor, the memory transistor being realized by a MOS transistor including a
15 memory gate oxide film that is arranged on a semiconductor substrate and a floating gate made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state, and the selection transistor being realized by a MOS transistor serially
20 connected to the memory transistor and including a selection gate oxide film that is arranged on the semiconductor substrate and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

a read circuit for switching on/off the fuse
25 MOS transistors according to the storage state of the

nonvolatile memory cell;

wherein at least one of the fuse MOS transistors
and the read circuit is configured as a peripheral circuit
transistor realized by a MOS transistor including a peripheral
5 circuit gate oxide film that is arranged on the semiconductor
substrate, and a peripheral circuit gate made of polysilicon
that is arranged on the peripheral circuit gate oxide film
which peripheral circuit gate oxide film is arranged to be
thicker than the memory gate oxide film.

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11. A semiconductor device comprising:

a constant voltage generating circuit that includes
an output driver that controls output of an input voltage, a
divider resistor circuit that divides an output voltage and
15 outputs the divided voltage, a reference voltage generating
circuit that generates a reference voltage, and a comparator
circuit that compares the divided voltage from the divider
resistor circuit with the reference voltage from the reference
voltage generating circuit and controls an operation of the
20 output driver according to the comparison result;

the divider resistor circuit including

a plurality of resistance value adjusting
resistor elements that are serially connected;

a plurality of fuse MOS transistors as the
25 fuse elements that are connected in parallel to the resistance

value adjusting resistor elements;

a nonvolatile memory cell that includes a memory transistor and a selection transistor, the memory transistor being realized by a MOS transistor including a memory gate oxide film that is arranged on a semiconductor substrate and a floating gate made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state, and the selection transistor being realized by a MOS transistor serially connected to the memory transistor and including a selection gate oxide film that is arranged on the semiconductor substrate and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

a read circuit for switching on/off the fuse MOS transistors according to the storage state of the nonvolatile memory cell;

wherein at least one of the fuse MOS transistors and the read circuit is configured as a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film which peripheral circuit gate oxide film is arranged to be thicker than the memory gate oxide film.

12. A semiconductor device comprising:

a semiconductor substrate;

a nonvolatile memory cell that includes

a memory transistor realized by a MOS

5 transistor including a memory gate oxide film that is arranged on the semiconductor substrate, and a floating gate made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state; and

a selection transistor realized by a MOS

10 transistor that is serially connected to the memory transistor, the selection transistor including a selection gate oxide film that is arranged on the semiconductor substrate, and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

15 a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film;

20 wherein an impurity concentration within the polysilicon of the floating gate is arranged to be lower than an impurity concentration within the polysilicon of the peripheral circuit gate oxide film.

25 13. The semiconductor device as claimed in claim 12,

wherein an impurity concentration within the polysilicon of the selection gate is equal to the impurity concentration within the polysilicon of the floating gate.

5 14. The semiconductor device as claimed in claim 12,
 wherein an impurity concentration within the polysilicon of the selection gate is equal to the impurity concentration within the polysilicon of the peripheral circuit gate.

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 15. The semiconductor device as claimed in claim 12,
 wherein the memory gate oxide film, the selection gate oxide film, and the peripheral circuit gate oxide film are arranged to have a same thickness.

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 16. The semiconductor device as claimed in claim 12,
 wherein the memory gate oxide film is arranged to be thinner than the peripheral circuit gate oxide film.

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 17. The semiconductor device as claimed in claim 16,
 wherein the selection gate oxide film and the memory gate oxide film are arranged to have a same thickness.

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 18. The semiconductor device as claimed in claim 16,
 wherein the selection gate oxide film and the

peripheral circuit gate oxide film are arranged to have a same thickness.

19. The semiconductor device as claimed in claim 12,
5 wherein the memory transistor and the selection
transistor are PMOS transistors.

20. A semiconductor device, comprising:
a divider resistor circuit that is configured to
10 obtain a voltage output through voltage division and adjust
the voltage output through cutting one or more fuse elements;
the divider resistor circuit including
a plurality of resistance value adjusting
resistor elements the are serially connected;
15 a plurality of fuse MOS transistors as the
fuse elements that are connected in parallel to the resistance
value adjusting resistor elements;
a nonvolatile memory cell that includes a
memory transistor and a selection transistor, the memory
20 transistor being realized by a MOS transistor including a
memory gate oxide film that is arranged on a semiconductor
substrate and a floating gate made of polysilicon that is
arranged on the memory gate oxide film which floating gate is
in an electrically floating state, and the selection
25 transistor being realized by a MOS transistor serially

connected to the memory transistor and including a selection gate oxide film that is arranged on the semiconductor substrate and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

5 a read circuit for switching on/off the fuse MOS transistors according to the storage state of the nonvolatile memory cell;

 wherein at least one of the fuse MOS transistors and the read circuit is configured as a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film, the polysilicon of the peripheral circuit gate being arranged
10 to have an impurity concentration that is higher than an
15 impurity concentration within the polysilicon of the floating gate.

21. A semiconductor device comprising:

20 a voltage detecting circuit that includes a divider resistor circuit that divides an input voltage and outputs the divided voltage, a reference voltage generating circuit that generates a reference voltage, and a comparator circuit that compares the divided voltage from the divider resistor circuit
25 with the reference voltage from the reference voltage

generating circuit;

the divider resistor circuit including

a plurality of resistance value adjusting
resistor elements that are serially connected;

5 a plurality of fuse MOS transistors as the
fuse elements that are connected in parallel to the resistance
value adjusting resistor elements;

a nonvolatile memory cell that includes a
memory transistor and a selection transistor, the memory
10 transistor being realized by a MOS transistor including a
memory gate oxide film that is arranged on a semiconductor
substrate and a floating gate made of polysilicon that is
arranged on the memory gate oxide film which floating gate is
in an electrically floating state, and the selection
15 transistor being realized by a MOS transistor serially
connected to the memory transistor and including a selection
gate oxide film that is arranged on the semiconductor
substrate and a selection gate made of polysilicon that is
arranged on the selection gate oxide film; and

20 a read circuit for switching on/off the fuse
MOS transistors according to the storage state of the
nonvolatile memory cell;

wherein at least one of the fuse MOS transistors
and the read circuit is configured as a peripheral circuit
25 transistor realized by a MOS transistor including a peripheral

circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film, the polysilicon of the peripheral circuit gate being arranged
5 to have an impurity concentration that is higher than an impurity concentration within the polysilicon of the floating gate.

22. A semiconductor device comprising:

10 a constant voltage generating circuit that includes an output driver that controls output of an input voltage, a divider resistor circuit that divides an output voltage and outputs the divided voltage, a reference voltage generating circuit that generates a reference voltage, and a comparator
15 circuit that compares the divided voltage from the divider resistor circuit with the reference voltage from the reference voltage generating circuit and controls an operation of the output driver according to the comparison result;

the divider resistor circuit including

20 a plurality of resistance value adjusting resistor elements that are serially connected;

a plurality of fuse MOS transistors as the fuse elements that are connected in parallel to the resistance value adjusting resistor elements;

25 a nonvolatile memory cell that includes a

memory transistor and a selection transistor, the memory transistor being realized by a MOS transistor including a memory gate oxide film that is arranged on a semiconductor substrate and a floating gate made of polysilicon that is
5 arranged on the memory gate oxide film which floating gate is in an electrically floating state, and the selection transistor being realized by a MOS transistor serially connected to the memory transistor and including a selection gate oxide film that is arranged on the semiconductor
10 substrate and a selection gate made of polysilicon that is arranged on the selection gate oxide film; and

a read circuit for switching on/off the fuse MOS transistors according to the storage state of the nonvolatile memory cell;

15 wherein at least one of the fuse MOS transistors and the read circuit is configured as a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon
20 that is arranged on the peripheral circuit gate oxide film, the polysilicon of the peripheral circuit gate being arranged to have an impurity concentration that is higher than an impurity concentration within the polysilicon of the floating gate.